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EXAMINER	
LANGMAN, JONATHAN C	

ART UNIT	PAPER NUMBER
1794	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/539,260	HAISMA, JAN	
	Examiner	Art Unit	
	JONATHAN C. LANGMAN	1794	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 December 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☒ Claim(s) *1-10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 June 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *6/15/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of Group I, claims 1-10, in the reply filed on December 13, 2007 and the cancellation of claims 11-20, drawn to group II are both acknowledged.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 1, the applicant uses the term "substantially" when referring to the dilation matching between the first material and the carrier material. It is unclear as to what range the applicant is attempting to claim with the limitation "substantially". How much is "substantially"?

Furthermore in regards to claim 1, in line 6, the applicant states "and having a dilation mismatch with the second material", the way that the claim is worded it is unclear as to what layer has the dilation mismatch. Does the first material mismatch the second material, or does the intermediate layer mismatch the second material? The examiner proposes changes: The applicant may insert a semicolon in line 5 after "first layer", and start a new paragraph with "wherein the first material"..." and furthermore

remove the comma separating "carrier material, and" in line 6, and finally make a new paragraph starting at "the intermediate layer having structures…".

Furthermore, regarding claim 1, the applicant has not defined what the limitation "structures" may entail. Can a structure be a solid layer? In claim 1, the applicant is essentially claiming a bonded wafer comprising two substrates (a carrier and a first layer) wherein the two substrates are separated by a intermediate layer (insulator), by definition a SOI wafer. Since the applicant has not defined "structure" in the sense of the claim, the insulator layer as a whole is construed to be a structure.

Claim 7 recites the limitation "the dimensions" in line 2. There is insufficient antecedent basis for this limitation in the claim. Furthermore, it is unclear as to what dimensions the applicant is claiming. Does the applicant mean thickness, width, height or all three?

Regarding claims 8 and 9, it is unclear as to how the structures lie in both perpendicular and parallel planes. Is the applicant attempting to claim a shape of the carrier, or perhaps a thickness of the structure? Regardless the structures are three dimensional, and the carrier substrate is three dimensional and therefore occupies an infinite amount of planes, or more specifically three planes x, y, or z. By describing the structures as lying perpendicular or parallel to "**a plane**" is irrelevant because the applicant has not defined these carrier planes, and therefore any structure on the surface of the carrier will be said to be lying perpendicular or parallel to any plane of the carrier material.

Claims 2-10 are rejected for being dependent upon a base rejected claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Haberger et al. (WO9967820), published December 29, 1999, whose US counterpart (US 6,417,075), is referenced as the English translation.

In regards to claims 1, 4, and 5, the applicant is essentially claiming a bonded wafer comprising two substrates (a carrier and a first layer) wherein the two substrates are separated by a intermediate layer (insulator), wherein the insulator has structures. Any SOI bonded wafer in the art would read on this claim, and if the insulator layer is patterned then it would read on all the instant dependent claims instantly set forth. Haberger et al. teach an SOI wafer comprising a first substrate and a second substrate bonded to each other by their faces via one or several intermediate bonding layers. At least one of the bonding layers is configured that it presents channel shaped recesses (col. 3, lines 62-66). The two substrates are preferably semiconductor substrates (col.

4, lines 5), and specifically mention the substrates to be silicon (see the entire specification). Two silicon wafers will have dilatation behaviors that are substantially the same, since they are the same material. The bonding layers are taught to be SiO_2 in preferred embodiments (col. 5, lines 1-8). A SiO_2 layer has a dilatation mismatch with the first layer (silicon). The patterned trenches are structures that expectantly and inherently absorb stress originating from the dilatation mismatch.

Regarding claims 2 and 3, the insulator (bonding) layers are taught to be buried oxide layers (col. 4, line 66), thus showing that the structures comprised of the insulating material further extend into the carrier. The trenches are formed of the same material and by the same process as instantly claimed (selective patterning with photolithography and then wet or dry etching), and therefore are expected to have the same structural features as instantly claimed.

Regarding claim 6, SiO_2 is electrically insulating.

Regarding claim 7, Haberger et al. teaches that the width of the trenches and height of the trenches is less than one centimeter (col. 6, lines 61-64).

Regarding claim 8, the channels have a linear orientation perpendicular to a plane of the carrier (col. 4, lines 38-39, and figures 2).

Regarding claim 9, the channels are rectangular in shape and extend across the wafer (figure 2), therefore, the structures are parallel to a plane of the carrier, as described in the 112 rejections above. Furthermore, Haberger et al. describe that the structures need not present a rectangular cross section, or across linear orientations

(col. 4, lines 38-43), therefore the channels may take on any shape desired, including those instantly claimed.

Regarding claim 10, the composite substrate is an SOI wafer.

Claims 1, 2, and 4-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Schrantz et al. (US 5,552,345).

Regarding claims 1, 2, 4-6, and 8-10, Schrantz et al. teach a silicon on insulator substrate wherein diamond is the insulator. As seen in Figures 2a-2b, a bonded structure comprising a silicon wafer 2, diamond layer 3 and device layer, 4, (silicon per col. 3, lines 43)shown. The diamond insulator layer is patterned and portions of it are selectively removed in order to define a series of scribe lines 6 (col. 4, lines 37-52). The streets, 6, may be left void (col. 4, line 26). The term "lines" of "scribe lines" also seen in figures 2a-2c denotes a linear formation, thus reading on instant claim 8, and the rectangular shape of instant claim 9. The two silicon wafers, 2 and 4 have the same dilation behavior, and diamond has a different dilatation behavior than that of the carrier. The diamond layer is formed into structures by patterning and etching, therefore showing that the structures extend through the thickness of the diamond layer, and will inherently and expectantly absorb stress originating from the dilatation mismatch.

Regarding claims 1, 2, and 4-10, Schrantz further teach another embodiment taught that reads upon the applicants instantly claimed structure; this structure is shown in Figures 4, specifically, figures 4c-4e, wherein 4e omits the sacrificial silicon wafer, 2, bonded to the bottom of layer 3. This structure comprises sacrificial wafer, 2, not

shown, SiO_2, insulating materials 26, patterned and distributed between the handle wafer and the device wafer 20, which also comprises silicon. The patterned SiO_2 material 26, will inherently and expectantly absorb the dilation mismatch between the device layer, 20, and the handle layer 2, or as a matter of fact any layer disposed there under. The SiO_2 layers have lateral size of 2-5 microns (col. 6, lines 4-24) and are in the shape of squares (fig. 4c) thus reading on instant claim 9. A square also is in the shape of a short line, thus reading on instant claim 8. Schrantz et al. teach that the sacrificial layer is removed, however this occurs after bonding. Therefore the instantly claimed structure is realized after bonding but before the removal of the sacrificial layer 2.

Regarding the orientation limitations of claims 8 and 9; by the applicant describing the structures as lying perpendicular or parallel to **"a plane"** is irrelevant because the applicant has not defined these carrier planes, and therefore any structure on the surface of the carrier will be said to be lying perpendicular or parallel to any plane of the carrier material.

Claims 1, 2, 4-6 and 9-10 are rejected under 35 U.S.C. 102(a) and 102 (e) as being anticipated by Chong et al. (US 6,544,863).

Chong et al. teach in Fig 2d, the instantly claimed structure. A substrate 201 that may be a semiconductor or silicon is covered with a layer of silicon dioxide 202, (an insulator). A stencil of the desired pattern may then be placed upon the insulating layer 202 to provide a patterned insulating layer on the silicon substrate 201. A substrate material 203, which is of the same material as the silicon layer 201, is then bonded to

the patterned side of the protective layer (col. 3, lines 50-67). The patterned structures of the silicon oxide layer expectantly and inherently absorb the dilation mismatch between the semiconductor substrates and the intermediate film, silicon dioxide. Regarding claim 9, as seen in figures 2c and 2d, the silicon oxide has a rectangular shape parallel to a plane of the carrier.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 9 is rejected under 35 U.S.C. 103(a) as being anticipated by Haberger et al. (WO9967820), published December 29, 1999, whose US counterpart (US 6,417,075), is referenced as the English translation, as applied above.

Haberger et al. teach a SOI substrate comprising two semiconductor wafers separated by a patterned oxide insulating layer of silicon dioxide, as described above. Haberger et al. teach shapes and sizes as seen in figures 2 and 3, and mentioned above, however do not teach all of the shapes instantly claimed, it would have been obvious to a person having ordinary skill in the art at the time the present invention was made and well within their grasps to choose any desired pattern including those shapes and sizes instantly claimed, as these are shown to be desired effective results. It would have been obvious to one having ordinary skill in the art at the time of the invention to

adjust the shapes and sizes of patterns in the insulating layer for the intended application, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Claims 3, and 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chong et al. (US 6,544,863), as applied above.

Chong et al. teach a SOI substrate comprising two semiconductor wafers separated by a patterned oxide insulating layer of silicon dioxide, as described above. Chong et al. is silent to the structures of the oxide layer extending into the handle wafer, however, buried oxide layers are well known in the art and obvious for using in SOI wafers. If a buried oxide insulating layer is used, and subsequently patterned by the methods of Chong et al., the structures would then extend into the handle or carrier substrate.

In regards to claims 7-9, Chong et al. teach that the insulating layer may be patterned as desired. It would have been obvious to a person having ordinary skill in the art at the time the present invention was made and well within their grasps to choose any desired pattern including those shapes and sizes instantly claimed, as these are shown to be desired effective results. It would have been obvious to one having ordinary skill in the art at the time of the invention to adjust the shapes and sizes of patterns in the insulating layer for the intended application, since it has been held that

discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The X references EP 1213748, EP 0809288, and Spiering et al. "Sacrificial wafer bonding for planarization after very deep wafer etching" all teach the structures being formed in the handle wafer and not being formed of the intermediate or insulating layer". The applicant is instantly claiming a SOI wafer wherein the insulator layer is selectively patterned; therefore more pertinent art was chosen to read upon the applicants' claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JONATHAN C. LANGMAN whose telephone number is (571)272-4811. The examiner can normally be reached on Mon-Thurs 6:30 am - 4:00 pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Callie Shosho can be reached on 571-272-1123. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JCL
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